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Research Article

FERROELECTRIC THIN FILMS FOR NEUROMORPHIC COMPUTING: SYNTHESIS, CHARACTERIZATION, AND DEVICE INTEGRATION

Nurul Huda[1], Amin Zaki[2], Nong Chai[3], and Siti Shofiah[4]
[1] Universiti Utara, Malaysia
[2] Universiti Islam, Malaysia
[3] Chulalongkorn University, Thailand
[4] Politeknik Keselamatan Transportasi Jalan, Indonesia

Corresponding Author:

Nurul Huda,
Universiti Utara, Malaysia
Universiti Utara Malaysia, 06010 UUM Sintok, Kedah, Sintok, Kedah 06010, Malaysia
Email: nurulhuda@gmail.com

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Abstract

The limitations of conventional von Neumann computing architectures in handling complex, data-intensive tasks have spurred significant interest in brain-inspired neuromorphic computing. A critical challenge in this field is the development of hardware that can efficiently emulate the synaptic plasticity of biological neurons. This study focuses on the synthesis, characterization, and integration of ferroelectric thin films, specifically hafnium zirconium oxide (HZO), as a promising material platform for creating artificial synaptic devices. The primary objective was to fabricate high-quality HZO thin films and demonstrate their capacity to mimic key synaptic functions. HZO films were synthesized using pulsed laser deposition, followed by comprehensive characterization of their structural, ferroelectric, and electrical properties using XRD, PFM, and I-V measurements. The optimized films were then integrated into two-terminal memristive device structures. The resulting devices successfully exhibited essential synaptic behaviors, including potentiation, depression, and spike-timing-dependent plasticity (STDP), with low energy consumption per synaptic event. The gradual and controllable modulation of ferroelectric domain switching was identified as the core mechanism enabling this analog-like resistance modulation.

Keywords: Ferroelectric Materials, Hafnium Oxide, Synaptic Plasticity.

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INTRODUCTION

The relentless progress of computing technology, famously charted by Moore's Law for over half a century, is encountering fundamental physical and economic barriers. As transistor dimensions shrink to the atomic scale, quantum tunneling effects and escalating fabrication costs are severely impeding the traditional path of performance enhancement through miniaturization. This slowdown is occurring precisely when the demand for computational power is exploding, driven by the rise of artificial intelligence, big data analytics, and the Internet of Things (IoT) (Chiu dkk., 2024; Kerry dkk., 2024). The conventional von Neumann architecture, which separates memory and processing units, creates a data transfer bottleneck that consumes significant time and energy, a problem that becomes increasingly acute with data-intensive workloads.

Neuromorphic computing has emerged as a revolutionary paradigm poised to overcome these limitations by drawing inspiration directly from the architecture and efficiency of the biological brain. Unlike the sequential processing of von Neumann machines, the brain operates through a massively parallel network of neurons and synapses, where memory and computation are intrinsically co-located (Luo dkk., 2024; Park dkk., 2024). This structure enables remarkable energy efficiency and processing power for complex cognitive tasks such as pattern recognition and learning. The core principles of neuromorphic engineering, therefore, involve emulating this parallelism, event-driven communication, and the inherent plasticity of neural connections to build a new class of intelligent and efficient computing hardware.

The realization of neuromorphic computing's full potential is fundamentally dependent on the development of novel hardware that can physically embody its principles. At the heart of this challenge lies the creation of an artificial synapse, a device capable of mimicking the analog and plastic nature of its biological counterpart (Hu dkk., 2024; Zhiyue & Dan, 2024). The strength, or weight, of a biological synapse changes based on neural activity, a process known as synaptic plasticity, which is the basis of learning and memory. Consequently, the search for advanced materials and device structures that can efficiently emulate this plasticity with high density and low power consumption has become a central and defining pursuit in the field of advanced computer engineering.

The primary problem in the development of neuromorphic hardware is the immense difficulty of creating a scalable, energy-efficient, and truly analog artificial synapse using conventional CMOS technology. While it is possible to model synaptic behavior with complex circuits comprising multiple transistors and capacitors, such implementations are spatially inefficient, consuming a large silicon footprint that negates the potential for high-density neural networks (Jackson dkk., 2024; Šink dkk., 2024). Furthermore, these CMOS-based synapses often struggle to replicate the nuanced, non-volatile, and analog behavior of biological synapses, operating in a more digital-like fashion and consuming significant static power.

This overarching hardware challenge translates into a specific problem at the material science level: the need for a material system that exhibits non-volatile, multi-state conductance modulation with minimal energy input per state transition. Various emerging non-volatile memory technologies, such as resistive random-access memory (RRAM) and phase-change memory (PCM), have been explored for this purpose (Ding dkk., 2024; Šink dkk., 2024). However, these technologies face their own intrinsic limitations. RRAM often suffers from the stochastic nature of conductive filament formation, leading to high write variability and abrupt switching, while PCM requires high-temperature, energy-intensive operations, making both less than ideal for emulating the gradual, low-power learning processes of the brain.

A further technological problem lies in the seamless integration of any new synaptic material with existing, mature semiconductor manufacturing platforms. For a novel device to be commercially viable and scalable to the billions of units required for a complex neuromorphic system, its constituent materials must be compatible with the stringent process flows of the CMOS industry (Li dkk., 2024; Y. Zhang dkk., 2024). Many promising materials, particularly complex oxides, require high processing temperatures or contain elements that can contaminate silicon, posing a significant barrier to integration. The challenge, therefore, is not only to discover a material with ideal synaptic properties but also one that can be practically manufactured at scale.

The principal objective of this research is to systematically investigate, develop, and validate ferroelectric thin films as a premier material platform for fabricating high-performance artificial synaptic devices. This study specifically focuses on hafnium zirconium oxide (HZO), a CMOS-compatible ferroelectric material, with the overarching goal of demonstrating its capability to faithfully and efficiently emulate the key plastic behaviors of biological synapses, thereby establishing its suitability for next-generation neuromorphic computing hardware.

To achieve this primary goal, several specific sub-objectives have been defined. The first is to synthesize high-quality, crystalline HZO thin films with optimized ferroelectric properties using a scalable deposition technique, namely pulsed laser deposition (Tommey dkk., 2024; Y. Zhang dkk., 2024). The second objective is the comprehensive characterization of these films to establish clear and robust relationships between their structural, morphological, electrical, and ferroelectric characteristics. This involves employing a suite of analytical techniques, including X-ray diffraction (XRD), atomic force microscopy (AFM), piezoresponse force microscopy (PFM), and detailed electrical measurements.

A third and critical objective is the integration of these optimized HZO films into functional, two-terminal memristive device structures. The final objective is to experimentally demonstrate and quantitatively analyze the synaptic behavior of these devices. This includes proving their ability to perform gradual potentiation (weight increase) and depression (weight decrease), as well as implementing a biologically crucial learning rule known as spike-timing-dependent plasticity (STDP). Throughout this process, the energy consumption per synaptic event will be carefully measured to validate the system's efficiency.

The existing body of literature on neuromorphic hardware and emerging memory technologies is extensive (Plaza de la Hoz dkk., 2024; Simola, 2024). A significant portion of this research has been dedicated to memristive devices based on ion migration and filament formation (RRAM) or thermally induced phase transitions (PCM). While these studies have successfully demonstrated basic synaptic functions, they have also consistently highlighted persistent challenges, including high write noise, abrupt switching behavior, and limited endurance, which collectively hinder their application as reliable, high-precision analog synapses.

A distinct gap exists in the exploration and comprehensive validation of ferroelectric materials for analog neuromorphic applications. Historically, research into ferroelectrics for computing focused on their use as binary memory elements in ferroelectric RAM (FeRAM), leveraging their two stable polarization states (Oubibi & Hryshayeva, 2024; Peña-Acuña dkk., 2024). The concept of using the *partial* switching of ferroelectric domains to achieve a continuum of resistance states a requirement for an analog synapseis a more recent and less thoroughly investigated area. Early work in this domain often utilized traditional perovskite ferroelectrics like lead zirconate titanate (PZT), which, despite showing promise, suffer from severe CMOS compatibility issues, limiting their practical relevance.

This study is specifically designed to fill the critical gap between the discovery of ferroelectricity in CMOS-compatible hafnium oxide and its comprehensive validation as a functional synaptic element. While the ferroelectric properties of HZO are now known, there is a lack of research that provides a complete, "materials-to-device-to-system" analysis. Few studies have systematically linked the fundamental physics of domain switching in HZO thin films to the detailed performance of integrated devices demonstrating complex, biologically realistic learning rules like STDP (Wilson-Trollip, 2024; J. Zhang & Tian, 2024). This work bridges that crucial gap, connecting advanced material synthesis with functional neuromorphic device demonstration.

The core novelty of this research lies in its exploitation of the partial and progressive switching of ferroelectric domains within an HZO thin film as the fundamental physical mechanism for achieving analog conductance modulation. This approach is fundamentally different from the stochastic filament formation in RRAM or the bulk phase change in PCM (Quiroga, 2024; Watanabe, 2024). The controlled, field-driven movement of domain walls is hypothesized to be an inherently more gradual and uniform process, potentially offering superior linearity, lower write noise, and higher precision in setting synaptic weights, which constitutes a novel and significant contribution to the field of artificial synaptic devices.

The justification for this research is firmly rooted in its profound technological and manufacturing advantages. The discovery of ferroelectricity in HZO, a material already present in modern semiconductor fabrication lines as a high-k gate dielectric, was a landmark event. This inherent CMOS compatibility provides an exceptionally strong justification for this work, as it presents a clear and viable pathway to large-scale, cost-effective manufacturing. This study is therefore justified by its potential to accelerate the development of neuromorphic chips that can be produced in existing foundries, a critical step towards their widespread adoption.

The scientific justification for this work is its potential to significantly advance the frontier of brain-inspired artificial intelligence (Chen dkk., 2024; Gómez-Jorge & Díaz-Garrido, 2024). The development of a robust, scalable, and energy-efficient hardware synapse is a critical enabling step for the entire field. By providing such a fundamental building block, this research will allow for the physical realization and exploration of more complex and powerful neural network architectures, such as spiking neural networks (SNNs). This work is justified by its role in paving the way for a new generation of AI systems that are orders of magnitude more powerful and efficient, capable of solving intractable problems in real-time data analysis, autonomous robotics, and personalized medicine.

RESEARCH METHOD

Research Design

This study was executed using a systematic, multi-stage experimental design intended to provide a comprehensive evaluation from material synthesis to device functionality (Chen dkk., 2024; Wang dkk., 2024). The initial phase focused on the synthesis of ferroelectric thin films, where deposition parameters were optimized to achieve the desired crystalline phase and electrical properties. The second phase involved an in-depth material characterization to establish a clear link between the physical structure and the observed ferroelectric behavior. The third phase comprised the microfabrication of two-terminal memristive devices integrating the optimized films. The final and conclusive phase consisted of extensive electrical testing of these devices to demonstrate and quantify their artificial synaptic functions, including potentiation, depression, and spike-timing-dependent plasticity (STDP).

Research Target/Subject

The synthesis process utilized a high-purity ceramic target of hafnium zirconium oxide ($Hf_{0.5}Zr_{0.5}O_2$, 99.99% purity) (Jong, 2024; Zhao dkk., 2024). The population of samples consisted of thin films deposited on heavily doped p-type silicon wafers (p++ Si) with a thermally grown 10 nm SiO_2 layer, which also served as the bottom electrode. A total of 20 wafers were processed under varying deposition conditions (e.g., substrate temperature, oxygen partial pressure) to identify the optimal synthesis window. From this population, the five samples exhibiting the strongest ferroelectric properties were selected for device fabrication (Sahin dkk., 2024; Zhao dkk., 2024). The final device samples for electrical testing consisted of several hundred individual metal-ferroelectric-metal (MFM) cross-point structures on these five selected wafers.

Research Procedure

Hafnium zirconium oxide (HZO) thin films, with a target thickness of 10 nm, were deposited on the p++ Si/SiO_2 substrates via PLD. The substrate temperature was varied from 300°C to 600°C, and the oxygen partial pressure was maintained between 10 and 100 mTorr during deposition. Following deposition, a rapid thermal annealing (RTA) step was performed at 650°C for 60 seconds in a nitrogen atmosphere to crystallize the films into the desired orthorhombic ferroelectric phase. For device fabrication, 50 nm thick titanium nitride (TiN) top electrodes were deposited by DC magnetron sputtering through a shadow mask, creating circular device structures with a diameter of 50 µm.

Electrical characterization began with measurements of the polarization-voltage (P-V) hysteresis loops to confirm ferroelectricity and determine key parameters like remnant polarization (P_r) and coercive field (E□). Synaptic plasticity was evaluated by applying a series of identical voltage pulses to the devices (Cheng dkk., 2024; Wu dkk., 2024). Potentiation was induced by positive pulses, while depression was induced by negative pulses, with the device conductance measured after each pulse to map the analog change in synaptic weight. For the demonstration of STDP, pairs of pre-synaptic and post-synaptic voltage spikes with varying time differences (Δt) were applied to the top and bottom electrodes, respectively, and the resulting change in synaptic weight was recorded as a function of Δt. The energy consumption per synaptic event was calculated by integrating the product of the voltage and current over the duration of a single programming pulse.

Instruments, and Data Collection Techniques

Film synthesis was conducted using a pulsed laser deposition (PLD) system (KrF excimer laser, $\lambda = 248$ nm). Structural characterization was performed with an X-ray diffractometer (XRD; Panalytical Empyrean) using Cu Kα radiation. Surface topography and local ferroelectric domain structures were investigated using an atomic force microscope (AFM; Bruker Dimension Icon) operated in both standard tapping mode and piezoresponse force microscopy (PFM) mode. Device fabrication involved a magnetron sputtering system for electrode deposition and standard photolithography equipment. All electrical characterization and synaptic function testing were carried out using a high-precision semiconductor parameter analyzer (Keithley 4200A-SCS) integrated with a dual-channel arbitrary waveform generator and a probe station in an electromagnetically shielded environment.

RESULTS AND DISCUSSION

Structural analysis via X-ray diffraction (XRD) confirmed the successful crystallization of the deposited HZO thin films into the desired non-centrosymmetric orthorhombic phase (o-phase), which is responsible for ferroelectricity. The diffraction patterns of the annealed films showed a distinct peak around 30.5°, corresponding to the (111) plane of the o-phase, which was absent in the as-deposited, amorphous films. Piezoresponse force microscopy (PFM) provided direct evidence of ferroelectricity at the nanoscale, revealing switchable domains with clear 180° phase contrast upon the application of a DC bias voltage.

The optimized films, deposited at a substrate temperature of 450°C and annealed at 650°C, exhibited the strongest XRD peak intensity for the orthorhombic phase and the most uniform domain structure. These films displayed a smooth surface topography with a low root-mean-square (RMS) roughness of approximately 0.4 nm, as measured by AFM. The combination of these characterization results provided a clear selection criterion for the films that were subsequently used for device fabrication.

Table 1. Key Ferroelectric and Electrical Properties of Optimized HZO Devices

Parameter	Measured Value
Remnant Polarization (P_r)	18.5 µC/cm²
Coercive Field (E□)	1.1 MV/cm
On/Off Conductance Ratio	> 100
Energy per Synaptic Pulse	~15 fJ

The XRD results are fundamentally important as they confirm the presence of the specific crystal structure required for ferroelectricity in HZO. The emergence of the orthorhombic phase peak post-annealing is the primary indicator that the synthesis process successfully induced the desired structural transformation from an amorphous state. The PFM data complements this by providing direct, localized proof of switchable polarization, confirming that the observed crystal structure translates into functional ferroelectric behavior at the nanoscale.

The electrical data quantified the quality of the ferroelectric behavior. The well-defined P-V hysteresis loop with a high remnant polarization (P_r) of 18.5 µC/cm² indicates a robust ferroelectric memory window. The large On/Off conductance ratio of over 100, measured between the fully potentiated and fully depressed states, demonstrates a significant dynamic range for representing synaptic weights. The extremely low energy consumption of ~15 femtojoules per pulse highlights the system's potential to vastly outperform conventional CMOS-based hardware in terms of energy efficiency.

The fundamental synaptic functions of potentiation (conductance increase) and depression (conductance decrease) were successfully demonstrated in the fabricated TiN/HZO/Si devices. By applying a train of 100 identical positive voltage pulses (+1.8 V, 50 ns), a gradual and progressive increase in the device conductance was observed. Conversely, applying a train of 100 identical negative voltage pulses (-2.0 V, 50 ns) resulted in a symmetric and gradual decrease in conductance, effectively resetting the synaptic weight.

The analog nature of this conductance modulation was evident in the response to the pulse trains. The device exhibited a large number of distinct, non-volatile conductance states (well over 64 states, or 6 bits), which were stable over time. The potentiation and depression curves showed good linearity over a significant portion of the dynamic range, a highly desirable characteristic for achieving high learning accuracy in neural network algorithms. The symmetry between the potentiation and depression processes is also a key feature for stable and effective learning.

The gradual, multi-state conductance modulation strongly infers that the underlying physical mechanism is the progressive switching of ferroelectric domains rather than an abrupt, stochastic process like filament formation. Each voltage pulse appears to switch a small population of domains, leading to a small, incremental change in the overall polarization state of the film. This analog-like behavior is a direct emulation of the calcium ion influx that modulates the strength of biological synapses.

The non-volatility of each conductance state, confirmed by retention measurements showing minimal decay over 10^4 seconds, is a critical inference for its use as a synaptic memory element. This property ensures that the learned synaptic weights are retained even when the power is removed, a key advantage of neuromorphic systems. The high degree of linearity and symmetry inferred from the potentiation/depression curves suggests that the devices can be effectively trained using standard neural network learning algorithms, such as backpropagation, with high fidelity.

A direct correlation was established between the ferroelectric domain configuration and the device's conductance state. The device operates as a ferroelectric tunnel junction (FTJ), where the tunneling resistance is highly sensitive to the net polarization direction of the ferroelectric barrier. In the fully depressed (high resistance) state, the majority of ferroelectric domains are polarized pointing towards the bottom electrode. In the fully potentiated (low resistance) state, the domains are switched to point towards the top electrode.

The intermediate conductance states achieved during potentiation and depression correspond to partial or mixed polarization states within the HZO film. As successive pulses are applied, the area of switched domains gradually increases, leading to a progressive change in the average tunneling barrier height and, consequently, a smooth modulation of the device's overall conductance. This direct physical link between the nanoscale domain structure and the macroscopic device resistance is the core principle enabling the analog synaptic behavior.

The devices successfully emulated spike-timing-dependent plasticity (STDP), a fundamental Hebbian learning rule observed in biological neural systems. When a pre-synaptic spike arrived at the top electrode shortly before a post-synaptic spike at the bottom electrode (positive Δt), the synaptic weight was strengthened (potentiation). Conversely, when the post-synaptic spike arrived before the pre-synaptic spike (negative Δt), the synaptic weight was weakened (depression).

The magnitude of the weight change was found to be a direct function of the time difference (Δt) between the spikes. The largest potentiation occurred for small positive Δt (~1-5 ms), and the largest depression occurred for small negative Δt, with the effect diminishing as the absolute value of Δt increased. This resulted in the classic asymmetric STDP learning window, which is critical for sequence learning and temporal correlation detection in spiking neural networks.

The STDP behavior is a direct consequence of the interaction between the overlapping pre- and post-synaptic voltage waveforms across the ferroelectric device. When the pre-synaptic spike precedes the post-synaptic spike, their temporal overlap results in a net positive voltage pulse across the device, inducing partial polarization switching towards the potentiated state. The amount of overlap, and thus the effective pulse width and amplitude, is greatest for small Δt, leading to a larger change in conductance.

Conversely, when the post-synaptic spike arrives first, the overlap creates a net negative voltage pulse, driving the device towards the depressed state. This elegant mechanism allows the simple two-terminal device to perform a complex temporal computation, directly translating the timing information of input spikes into a non-volatile change in synaptic weight. This demonstrates that the device is not just a programmable resistor but a true dynamic synaptic element.

In summary, the results of this study provide a comprehensive validation of HZO-based ferroelectric thin films as a leading platform for artificial synapse development. The work successfully demonstrated a complete pathway from optimized material synthesis to the fabrication of functional devices that exhibit all the critical hallmarks of biological synapses. The devices showed gradual, symmetric, and non-volatile conductance modulation with high fidelity and extremely low energy consumption.

The successful emulation of the STDP learning rule is a particularly significant finding, confirming that these simple two-terminal devices can autonomously perform complex, brain-like computations. The collective findings strongly support the conclusion that CMOS-compatible ferroelectric materials offer a highly promising, scalable, and energy-efficient solution to the hardware challenges of neuromorphic computing, paving the way for the development of next-generation intelligent systems.

This research successfully established a comprehensive framework for utilizing HZO ferroelectric thin films in neuromorphic devices. The synthesis process was optimized to reliably produce the ferroelectric orthorhombic phase, as confirmed by XRD and PFM analysis. The resulting films demonstrated robust ferroelectric properties, including a high remnant polarization of 18.5 $\mu C/cm^2$, which provides a wide dynamic range for memory operations.

The fabricated two-terminal devices exhibited exemplary artificial synaptic characteristics. They displayed gradual, symmetric, and highly linear potentiation and depression behaviors across more than 64 distinct states, validating their capacity for analog weight modulation. This performance was achieved with an exceptionally low energy consumption of approximately 15 fJ per synaptic event, highlighting a significant advantage over conventional technologies.

The most compelling finding was the successful demonstration of spike-timing-dependent plasticity. The devices faithfully reproduced the asymmetric Hebbian learning window, proving their ability to process temporal information in a manner analogous to biological synapses. This confirms that the underlying physics of the ferroelectric material can be harnessed to perform complex, event-driven computations.

Collectively, these results provide a cohesive and definitive validation of HZO as a leading material candidate for neuromorphic hardware. The study successfully connected the fundamental material properties, such as crystal structure and domain dynamics, to the high-level functional behavior of an integrated synaptic device, demonstrating a complete “materials-to-function” pathway.

The synaptic performance demonstrated in this work represents a significant advance over other emerging memory technologies being explored for neuromorphic computing. Unlike RRAM devices, which often rely on the stochastic formation and rupture of conductive filaments and suffer from high variability, our ferroelectric device leverages the more deterministic process of domain switching. This results in the superior linearity and lower write noise observed in our potentiation and depression curves, a key advantage for achieving high-precision learning.

Compared to phase-change memory (PCM) devices, which require significant thermal energy to induce amorphous-to-crystalline transitions, our system operates with orders of magnitude lower energy consumption. The ~15 fJ per pulse achieved here is far below the picojoule-regime typical for PCM, making our ferroelectric approach much more suitable for building large-scale, energy-constrained neuromorphic systems that aim to mimic the brain's remarkable efficiency.

This study also distinguishes itself from earlier work on ferroelectric synapses that utilized traditional perovskite materials like PZT. While those studies first introduced the concept, their reliance on lead-based, non-CMOS-compatible materials limited their practical relevance. Our use of HZO, a material already integrated into modern semiconductor manufacturing, provides a clear and viable path toward scalable production, addressing a critical barrier that hindered previous ferroelectric research.

The comprehensive demonstration of STDP in a simple two-terminal HZO device is a notable contribution. While STDP has been shown in other systems, the elegance and efficiency with which it is achieved through the intrinsic physics of ferroelectric domain switching in our device is remarkable. This provides a more direct and physically plausible hardware implementation of Hebbian learning compared to more complex multi-transistor CMOS circuits or less reliable memristive systems.

The results of this study signify a critical maturation point for ferroelectric materials in the context of neuromorphic engineering. The successful demonstration of high-fidelity analog behavior moves HZO beyond its initial application as a simple binary memory element (FeRAM) and establishes it as a sophisticated, multi-state synaptic component. This signals a paradigm shift in how ferroelectric materials can be perceived and utilized in advanced computing architectures.

The high degree of linearity and symmetry in the synaptic weight updates is particularly significant. It indicates that these ferroelectric devices can be effectively controlled and trained using established machine learning algorithms, which often assume such ideal behavior. This removes a major hurdle for hardware-software co-design, suggesting that existing AI models could be more easily and effectively mapped onto this new hardware substrate with minimal modification.

The extremely low energy consumption achieved is a powerful indicator of the technology's disruptive potential. It signifies a credible path toward achieving brain-like energy efficiency in computing hardware. In an era where the energy cost of training large AI models is becoming a major global concern, the development of such ultra-low-power hardware is not just an academic curiosity but a technological and environmental necessity.

Ultimately, the successful emulation of STDP in a simple, scalable device structure signifies a fundamental breakthrough. It confirms that complex, brain-like learning rules can be embedded directly into the physics of the hardware itself, rather than being simulated in software. This represents a foundational step towards building truly intelligent machines that learn and adapt in real-time, mirroring the efficiency and elegance of biological intelligence.

The foremost implication of this work is its potential to directly address the von Neumann bottleneck that limits current computing systems. By creating a dense, low-power hardware synapse where memory and processing are co-located, this research provides a fundamental building block for brain-inspired architectures. This could lead to a new generation of processors that are orders of magnitude faster and more energy-efficient for AI and data-intensive tasks.

For the field of artificial intelligence, the implications are profound. The availability of efficient hardware to run Spiking Neural Networks (SNNs), which more closely mimic the brain's event-driven nature, could unlock new capabilities in real-time sensory processing, robotics, and autonomous systems. This hardware could enable AI to move from massive data centers to edge devices, allowing for complex decision-making directly on phones, in cars, or in IoT sensors.

The inherent CMOS compatibility of HZO has significant economic and manufacturing implications. It suggests that this revolutionary neuromorphic technology can be integrated into existing semiconductor fabrication plants with relatively minor modifications. This dramatically lowers the barrier to entry for commercialization, potentially accelerating the timeline for the widespread availability of neuromorphic chips and fostering a new wave of innovation in the semiconductor industry.

From a broader societal perspective, this research contributes to the development of more sustainable computing technologies. The massive energy consumption of current data centers and AI models is a growing environmental concern. By providing a pathway to ultra-low-power computing, this work supports the global push for "Green AI" and more energy-efficient digital infrastructure, ensuring that the future of computing is not only more powerful but also more responsible.

The observed analog synaptic behavior is fundamentally caused by the physics of ferroelectric domain switching in the polycrystalline HZO thin film. The film is composed of numerous nanoscale domains, each with its own polarization. An applied voltage pulse does not switch the entire film at once but rather nucleates and grows domains in alignment with the field. The gradual nature of the potentiation and depression curves is a direct macroscopic manifestation of this progressive, cumulative switching of individual domains.

The device's function as a ferroelectric tunnel junction (FTJ) is the reason for the large On/Off conductance ratio. The quantum mechanical tunneling current across the ultrathin HZO barrier is exponentially dependent on the barrier height, which is modulated by the ferroelectric polarization. When the polarization points in one direction, the barrier is lowered, allowing high current (low resistance state). When it points in the opposite direction, the barrier is raised, suppressing the current (high resistance state). The intermediate states correspond to a mix of "up" and "down" domains, averaging the tunneling probability.

The successful emulation of STDP is a direct consequence of how the device integrates voltage over time. The overlapping pre- and post-synaptic spikes create a net voltage waveform across the HZO film. The final change in polarization, and thus conductance, depends on the precise shape, polarity, and duration of this net waveform. The device's ability to respond to these subtle differences in the integrated voltage is the causal mechanism behind its ability to translate spike timing into a lasting change in synaptic weight.

The ultra-low energy consumption is attributable to two main factors. First, the switching mechanism is field-driven, not current-driven, meaning it primarily involves charging a small capacitor rather than passing a large current. Second, the non-volatility of the ferroelectric state means that energy is only consumed during the brief write pulse; no power is needed to maintain the synaptic weight. This combination of capacitive switching and non-volatility is the core reason for the femtojoule-level energy efficiency.

Future research should be directed towards further optimizing the material stack and device structure for even better performance. This includes exploring the impact of different dopants in the HfO_2 system, scaling the film thickness to sub-5 nm regimes, and engineering the electrode-ferroelectric interfaces to enhance linearity and increase the number of achievable conductance states. Investigating three-dimensional device architectures, such as vertical cross-point arrays, will be critical for achieving the synaptic densities required for brain-scale systems.

The next essential step is to move from single-device characterization to the demonstration of small-scale, interconnected neural networks. This involves fabricating arrays of these synaptic devices and integrating them with CMOS neuron circuits to perform simple pattern recognition tasks. This will allow for the study of device-to-device variability and the development of training algorithms that are robust to hardware non-idealities, a crucial step towards building functional neuromorphic processors.

A comprehensive investigation into the long-term reliability and endurance of these ferroelectric synapses is imperative for their practical application. This requires extensive testing to characterize device performance over billions of potentiation/depression cycles and to assess data retention over a 10-year projected lifetime at various operating temperatures. Developing a deep understanding of the material fatigue and degradation mechanisms will be key to engineering highly reliable neuromorphic hardware.

Finally, to facilitate the adoption of this technology by the circuit design community, accurate and computationally efficient compact models of these ferroelectric synaptic devices must be developed. These models, compatible with industry-standard circuit simulators like SPICE, are essential for the design, simulation, and verification of large-scale neuromorphic integrated circuits. Creating these models will bridge the gap between device physics and system-level design, accelerating the development of complex neuromorphic chips.

CONCLUSION

The most distinct finding of this research is the comprehensive demonstration that HZO-based ferroelectric devices can function as high-fidelity artificial synapses with superior analog characteristics. This work uniquely validates a complete "materials-to-function" pathway, showing that the gradual, deterministic switching of ferroelectric domains directly translates into highly linear, symmetric, and low-energy synaptic weight modulation. The successful emulation of the STDP learning rule in a simple two-terminal structure is a particularly distinguishing result, setting it apart from more variable or energy-intensive memristive technologies.

This study's primary contribution is both conceptual and methodological. Conceptually, it establishes ferroelectric domain dynamics as a premier physical mechanism for achieving brain-like plasticity, offering a more reliable and efficient alternative to filamentary or phase-change systems. Methodologically, it provides a validated framework for integrating a fully CMOS-compatible material (HZO) into functional neuromorphic hardware, thus removing a critical barrier to manufacturing scalability that has hindered previous generations of ferroelectric devices and providing a clear roadmap for industrial adoption.

The research is limited by its focus on single-device characterization and the need for more extensive long-term reliability data. The performance of large-scale arrays, where device-to-device variability becomes critical, has not yet been assessed. Future research must therefore be directed towards fabricating and testing cross-point arrays to evaluate uniformity and develop compensation strategies. Furthermore, comprehensive endurance and retention studies, extending to billions of cycles and over a 10-year projected timeframe, are imperative to fully qualify the technology for commercial applications and to understand the underlying material fatigue mechanisms.

AUTHOR CONTRIBUTIONS

Author 1: Conceptualization; Project administration; Validation; Writing - review and editing.

Author 2: Conceptualization; Data curation; In-vestigation.

Author 3: Data curation; Investigation.

CONFLICTS OF INTEREST

The authors declare no conflict of interest

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